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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application 09/742,204	Applicant(s) FOX ET AL.	
	Examiner Khiem D Nguyen	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,19-24 and 27-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19-24 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02-27-2003 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

   (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Miyazawa et al. (U.S. Patent 5,953,619) and Evans et al. (U.S. Patent 6,150,184).

   AAPA teaches a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of (see the Background of the Invention on pages 1-4 of this application):

deposition of an electrically conductive bottom electrode layer (page 3, lines 29-30);

deposition of a layer of ferroelectric dielectric material, wherein the ferroelectric dielectric layer is comprises PZT (page 3, lines 31-33);

annealing the layer of ferroelectric dielectric material with a first anneal (page 4, lines 3-6);

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed by rapid thermal annealing (page 4, lines 7-9); and

deposition of an electrically conductive top electrode layer (page 4, line 10).

AAPA teaches doing the rapid thermal annealing before the formation of the top electrode but fails to teach doing the rapid thermal annealing after the formation of the top electrode as recited in present claims 1.

Miyazawa teaches doing the rapid thermal annealing before or after the upper electrode layer is deposited (col. 4, line 66 to col. 5, line 8). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Miyazawa's teaching into AAPA's method because in doing so the PZT dielectric film can be polycrystallized (col. 5, lines 9-10).

AAPA fails to explicitly disclose annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal and wherein the second anneal changing the layer of ferroelectric material into grains having a columnar structure as recited in present claim 1.

Miyazawa discloses annealing the layer of ferroelectric dielectric material to form perovskite phases (col. 1, lines 27-35) with a first anneal and wherein the second anneal (col. 4, line 66 to col. 5, line 8) changing the layer of ferroelectric material into grains having a columnar structure (col. 5, lines 9-16). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Miyazawa to enable the ferroelectric material of AAPA to be formed.

AAPA fails to teach etching the electrically conductive top electrode layer and annealing the layer of ferroelectric dielectric material with another anneal after etching the electrically conductive top electrode layer as recited in present claim 1.

Evans teaches etching the top electrode layer and annealing the layer of ferroelectric layer after etching the top electrode layer (col. 7, lines 48-56). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Evans's teaching into AAPA's method because in doing so the electrical switching performance of the ferroelectric capacitors can be improved (col. 2, lines 1-7).

3. Claims 2-3 and 5-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Miyazawa et al. (U.S. Patent 5,953,619) and Evans et al. (U.S. Patent 6,150,184) as applied to claims 1 and 4 above, and further in view of Joshi et al. (U.S. Patent 6,322,849) and Van Buskirk et al. (U.S. Patent 6,316,797).

AAPA fails to teach that the electrically conductive bottom electrode layer comprises a noble metal and wherein the electrically conductive bottom electrode layer comprises platinum as recited in claims 2 and 3.

Joshi teaches that the electrically conductive bottom electrode layer comprises platinum and palladium (col. 5, lines 11-15). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use platinum as bottom electrode material in the method of AAPA because platinum can provide electrode or contact function.

AAPA fails to teach that the electrically conductive top electrode layer comprises a noble metal oxide and wherein the electrically conductive top electrode layer comprises iridium oxide as recited in present claims 5 and 6.

Van Buskirk teaches that top electrode comprises of iridium oxide (col. 21, lines 5-10). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use iridium oxide as top electrode material in the method of AAPA because iridium oxide can provide electrode or contact function.

AAPA teaches the first and second annealing is done at a temperature and for time duration but fails to teach the ranges for the annealing temperature and time duration as recited in present claims 7-11.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal ranges for the annealing temperature and time duration through routine experimentation and optimization to obtain optimal or desired device performance because the annealing temperature and time duration are result-effective variables and there is no evidence indicating that the annealing temperature and time duration are critical and it has been held that it is not

inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

4. Claims 12-17 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Miyazawa et al. (U.S. Patent 5,953,619) and Otto et al. (U.S. Patent 6,284,712).

AAPA teaches a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of (see the Background of the Invention on pages 1-4 of this application):

deposition of an electrically conductive bottom electrode layer comprising a noble metal (page 3, lines 29-30);

deposition of a layer of ferroelectric dielectric material, wherein the ferroelectric dielectric layer is comprises PZT and performed by sputtering (page 3, lines 31-33);

annealing the layer of ferroelectric dielectric material with a first anneal (page 4, lines 3-6);

deposition of an electrically conductive top electrode layer comprising a noble metal oxide (page 4, line 10);

depositing an encapsulation layer; and,

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed by rapid thermal annealing (page 4, lines 7-9);

AAPA teaches doing the rapid thermal annealing before the formation of the top electrode but fails to teach doing the rapid thermal annealing after the formation of the top electrode as recited in present claim 12.

Miyazawa teaches doing the rapid thermal annealing before or after the upper electrode layer is deposited (col. 4, line 66 to col. 5, line 8). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Miyazawa's teaching into AAPA's method because in doing so the PZT dielectric film can be polycrystallized (col. 5, lines 9-10).

AAPA fails to explicitly disclose annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal and wherein the second anneal changing the layer of ferroelectric material into grains having a columnar structure as recited in present claim 12.

Miyazawa discloses annealing the layer of ferroelectric dielectric material to form perovskite phases (col. 1, lines 27-35) with a first anneal and wherein the second anneal (col. 4, line 66 to col. 5, line 8) changing the layer of ferroelectric material into grains having a columnar structure (col. 5, lines 9-16). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Miyazawa to enable the ferroelectric material of AAPA to be formed.

AAPA fails to teach that the first and second anneal is performed in an environment comprising a mixture of oxygen and inert gas as recited in present claims 12 and 15-20.

Otto teaches that the annealing process is performed in an environment comprising a mixture of inert gas and oxygen (col. 14, lines 59-64). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to performed

the first anneal in an environment comprising a mixture of oxygen and inert gas because doing so the desired total oxygen pressure can be obtained (col. 14, lines 59-65).

AAPA fails to teach the ranges for the partial pressure of oxygen and the annealing temperature as recited in claims 12, 15-16, 19 and 22.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal ranges for the partial pressure of oxygen and the annealing temperature through routine experimentation and optimization to obtain optimal or desired device performance because the partial pressure of oxygen and the annealing temperature are result-effective variables and there is no evidence indicating that the partial pressure of oxygen and the annealing temperature are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

5. Claims 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Miyazawa et al. (U.S. Patent 5,953,619) and Van Buskirk et al. (U.S. Patent 6,316,797).

AAPA teaches a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of (see the Background of the Invention on pages 1-4 of this application):

deposition of an electrically conductive bottom electrode layer comprising a noble metal (page 3, lines 29-30);

deposition of a layer of ferroelectric dielectric material, wherein the ferroelectric dielectric layer is comprises PZT and performed by sputtering (page 3, lines 31-33);

annealing the layer of ferroelectric dielectric material with a first anneal (page 4, lines 3-6);

deposition of an electrically conductive top electrode layer comprising a noble metal oxide (page 4, line 10); and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed by rapid thermal annealing (page 4, lines 7-9).

AAPA teaches doing the rapid thermal annealing before the formation of the top electrode but fails to teach doing the rapid thermal annealing after the formation of the top electrode as recited in present claims 27 and 30.

Miyazawa teaches doing the rapid thermal annealing before or after the upper electrode layer 29a is deposited (col. 4, line 66 to col. 5, line 8 and FIGS 10-12). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Miyazawa's teaching into AAPA's method because in doing so the PZT dielectric film can be polycrystallized (See col. 5, lines 9-10).

AAPA fails to explicitly disclose annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal and wherein the second anneal changing the layer of ferroelectric material into grains having a columnar structure as recited in present claims 27 and 30.

Miyazawa discloses annealing the layer of ferroelectric dielectric material to form perovskite phases (col. 1, lines 27-35) with a first anneal and wherein the second anneal

(col. 4, line 66 to col. 5, line 8) changing the layer of ferroelectric material into grains having a columnar structure (col. 5, lines 9-16). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Miyazawa to enable the ferroelectric material of AAPA to be formed.

AAPA fails to teach that the electrically conductive top electrode layer comprises a noble metal oxide and wherein the electrically conductive top electrode layer comprises iridium oxide as recited in present claims 29 and 30.

However, Van Buskirk teaches that top electrode comprises of iridium oxide (See col. 21, lines 5-10). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use iridium oxide as top electrode material in the method of AAPA because iridium oxide can provide electrode or contact function.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaudhuri Olik can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
March 21, 2003

George Fourson
Primary Examiner
2823